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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/062,143	GAD S. SHEAFFER	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-16,18-27 and 29-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-16,18-27 and 29-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 08/29/2007.

2. Claims 1-5, 7-16, 18-27, and 29-33 are pending in this application. Claims 1, 10, and 21 are independent claims. In Amendment, claims 6, 17, and 28 are cancelled. This Office Action is made final.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-5, 7-16, 18-27, and 29-33 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-5, 7-16, 18-27, and 29-33 cite a method, apparatus, and system for performing MAC according to a predetermined mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-5, 7-16, 18-27, and 29-33 merely disclose steps/components for performing MAC without disclosing a practical application or a useful and tangible result of MAC since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble

so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. Therefore, claims 1-5, 7-16, 18-27, and 29-33 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5, 7-8, 10-16, 18-19, 21-27, 29, and 31-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Sih et al. (U.S. 6,606,700).

Re claim 1, Sih et al. disclose in Figures 1-5 a method (e.g. a new DSP architecture as seen in abstract, generally Figure 1, and col. 3 lines 35-56) comprising:

receiving input data at an execution unit within a processor (e.g. input data into MACs from register file with labels PO1-PO6 as seen in Figure 1; the processor is the digital signal processor as seen in Figure 1 architecture; the execution unit generally comprises multiple MAC units as seen in Figure 1);

the execution unit (e.g. the execution unit generally comprises multiple MAC units as seen in Figure 1) performing one or more current multiply-accumulate operations on the received input data (e.g. MAC1-MAC4 are performed multiply-accumulate operations wherein the input data are from PO1 to PO6 as seen in Figure 1 and its mathematical representation is seen in Figure 3 as type of operation) with one or more modular multiply-accumulate units (e.g. MAC1-MAC4 as units) that are dynamically reconfigurable based on bandwidth requirements of the one or more multiply accumulate operations (e.g. abstract lines 1-3 and col. 3 line 58 to col. 4 line 8 wherein the MACs are programmable as needed to speedup the process by increasing the bandwidth of processing the input data); and

saving the received input data at one or more buffers (e.g. IS1 122 and IS2 138 are buffers to receive input data PO3, PO4, or delay version of that as seen in Figure 1) within the execution unit for one or more multiply-accumulate operations to be performed during a subsequent computational cycle (e.g. col. 3 lines 5-32 wherein MAC1 with MAC2 operate in one cycle and MAC3 with MAC4 can operate in another cycle) after the current multiply-accumulate operation (e.g. the current MACs as MAC1 and MAC2 in Figure 1).

Re claim 2, Sih et al. further disclose in Figures 1 and 3 the receiving comprises receiving first and second data by the execution unit (e.g. PO2 and PO3 from register file as the first and second data in Figure 1); and wherein the performing comprises performing by the execution unit a multiply-accumulate operation on the received first and second data (e.g. MAC1 with 104 and 118 as multiplier and accumulator

respectively) and a multiply-accumulate operation (e.g. MAC3 with 128 and 132 as multiplier and accumulator respectively) on the received first data and on input data saved by the execution unit (e.g. wherein the input data for MAC3 is PO2 and IS1 respectively as first data and saved data).

Re claim 3, Sih et al. further disclose in Figures 1 and 3 the receiving comprises receiving first, second, third, and fourth data by the execution unit (e.g. PO2-PO5 as first, third, second, and fourth data respectively input into MAC1-MAC4); and wherein the performing comprises performing by the execution unit a multiply-accumulate operation on the received first and third data (e.g. by MAC1), a multiply-accumulate operation on the received second and fourth data (e.g. by MAC2), a multiply-accumulate operation on the received first and fourth data (e.g. by MAC3), and a multiply-accumulate operation on the received second data and on input data saved by the execution unit (e.g. by MAC4).

Re claim 4, Sih et al. further disclose in Figures 1 and 3 the performing the multiply-accumulate operation on the received first and third data (e.g. by MAC1 in Figure 1) and the multiply-accumulate operation on the received second and fourth data (e.g. by MAC2 in Figure 1) comprise multiplying the received first and third data to produce a first product (e.g. output of 104), multiplying the received second and fourth data to produce a second product (e.g. output of 106), and adding (e.g. by adder 114) the first product (e.g. 108), the second product (e.g. 110), and an accumulated sum (e.g. MAC1).

Re claim 5, Sih et al. further disclose in Figures 1 and 3 saving by the execution unit received input data for one or more multiply-accumulate operations to be performed by the execution unit after the current multiply-accumulate repeating the receiving, performing, and saving by the execution unit one or more t m to accumulate data; and outputting the accumulated data by the execution unit (e.g. Figure 1 and col. 4 lines 19-26).

Re claim 7, Sih et al. further disclose in Figures 1 and 3 one or more tap coefficients are each a complex number and one or more input data samples are each a complex number (e.g. col. 4 lines 60-65).

Re claim 8, Sih et al. further disclose in Figures 1 and 3 saving by the execution unit saved input data for one or more multiply-accumulate operations to be performed by the execution unit (e.g. saving by the IS1 122 and IS2 138 in Figure 1).

Re claim 10, it is an apparatus claim of claim 1. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 11, it is an apparatus claim of claim 2. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 12, Sih et al. further disclose in Figures 1 and 3 the execution unit block comprises a single multiplier-accumulator comprising a multiplier to multiply the received first and second input data to produce a product (e.g. MAC3 with 128 as multiplier to produce first product), an accumulator to store an accumulated sum (e.g. 134), and an adder (e.g. 132) to add the product to the accumulated sum.

Re claim 13, it is an apparatus claim of claim 3. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 14, it is an apparatus claim of claim 4. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 15, Sih et al. further disclose in Figures 1 and 3 the execution unit block comprising one or more execution unit building blocks (e.g. MAC1-MAC4) each comprising one or more multiplier-accumulators and one or more buffers (e.g. IS1 and IS2).

Re claim 16, Sih et al. further disclose in Figures 1 and 3 the control logic to control the execution unit block to repeat, one or more times, receiving input data at one or more of the inputs (e.g. col. 2 lines 55-59), performing multiply- accumulate operations on the received input data and on input data stored in one or more buffers pf the execution unit block to accumulate data, and saving the received input data in one or more buffers of the execution unit block (Figure 1 and col. 4 lines 19-26).

Re claim 18, it is an apparatus claim of claim 7. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 19, it is an apparatus claim of claim 8. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 21, it is a system claim of claim 10. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 10. Further, Sih et al. disclose in Figure 1 and 3 a system comprising: a coder/decoder to receive analog signals

and convert the analog signals into corresponding input data (col. 1 lines 10-25 as DA converter).

Re claim 22, it is a system claim of claim 11. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 23, it is a system claim of claim 12. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 24, it is a system claim of claim 13. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 25, it is a system claim of claim 14. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Re claim 26, it is a system claim of claim 15. Thus, claim 26 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

Re claim 27, it is a system claim of claim 16. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 29, it is a system claim of claim 19. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 19.

Re claim 31, Sih et al. further disclose in Figures 1 and 3 performing is to implement a finite impulse response filter (e.g. abstract line 3) with the received input data comprising one or more tap (e.g. Figure 1 and col. 4 lines 19-26) and one or more input data samples and with the accumulated data in the accumulator comprising one or more output data samples (e.g. MAC1-MAC4).

Re claim 32, it is an apparatus claim of claim 31. Thus, claim 32 is also rejected under the same rationale as cited in the rejection of rejected claim 31.

Re claim 33, it is a system claim of claim 32. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 32.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9, 20, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sih et al. (U.S. 6,606,700) in view of Agarwal et al. (U.S. 5,825,677).

Re claim 9, Sih et al. fail to disclose in Figures 1 and 3 performing the receiving and performing in accordance with a single instruction multiple data instruction. However, Agarwal et al. disclose in Figures 4-5 the instruction is SIMD (e.g. col. 2 lines 1-50). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add performing the receiving and performing in accordance with a single instruction multiple data instruction as seen in Agarwal et al.'s invention into Sih et al.'s invention because it would enable to increase speed (e.g. col. 2 lines 10-15).

Re claim 20, it is an apparatus claim of claim 9. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 30, it is a system claim of claim 20. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 20.

Response to Arguments

9. Applicant's arguments filed 08/29/2007 have been fully considered but they are not persuasive.

a. The applicant argues in page 10 last paragraph for all claims rejected under 35 U.S.C. 101 that all the claims are directed to a practical/physical application since the processes implemented by an execution unit and other components within a processor as cited in the claimed invention.

The examiner respectfully submits that the processes as multiplication and accumulation implemented by an execution unit within a processor cannot constitute as a practical/physical application. The claims do not disclose any practical application as alleged by the applicant. At most, the claims only briefly disclose a multiply-accumulate operation in the execution unit with buffers to store the result of MAC without disclosing any practical application of the MAC operation in the execution unit with buffer as alleged by the applicant.

b. The applicant repeatedly and extensively argues in pages 11-12 for claims rejected under 35 U.S.C. 102(e) that the cited references fail to discloses an execution

unit having buffers to save data to perform multiply-accumulate operations during a subsequent computational cycle and further fail to disclose these elements being located within an execution unit to store input data received at the execution.

The examiner respectfully submits that the cited reference by Sih et al. clearly and expressively disclose in Figures 1-5 the execution unit having buffers to save data to perform multiply-accumulate operations during a subsequent computational cycle, particularly Figure 1 as general architecture of all embodiments, wherein MAC 4 operates on the saved data of MAC 3. The saved buffers IS1 and/or IS2 in Figure 1 is used to temporary store the input data for next cycle execution, similar to Figures 6-8 of the application. In addition, every MACs with appropriated buffer in Figure 1 is considered as an execution unit. In addition, Figure 2 clearly discloses the limitations an execution unit having buffers to save data to perform multiply-accumulate operations during a subsequent computational cycle (e.g. col. 4 lines 8-33) wherein each inputs into the corresponding MAC is delayed by storing in buffer by one cycle as expressively seen in Figure 2 and expressions in lines 15-28.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

October 11, 2007